What is claimed is:

1. A built-in jitter measurement circuit for a voltage-controlled oscillator (VCO) and a phase-locked loop (PLL) comprising:

a divider for dividing frequency of a signal to be measured by n;

a state controller as a controller for other components;

a variance calculator for calculating variance of the signal to be measured;

a mean calculator for calculating mean of the signal to be measured;

a time to digital converter (TDC) for converting the period of the signal to be measured into digital values; and

a encoder and counter for counting and encoding the digital values output from TDC;

wherein, the divider divides the frequency of the signal to be measured, the period of the divided signals to be measured are converted into digital values by TDC, encoder and counter, the digital values are calculated by the variance calculator and the mean calculator, and period means and jitter of the divided signal are determined.

2. The circuit of claim 1, wherein after the period mean and the jitter of the divided signal are determined, the circuit further comprises a step of performing calculation according to the equation as following:

$$Y' = \{y_1 + e_1, y_2 + e_2, y_3 + e_3, ...\}$$
$$M_{Y'} = nM_X + M_E$$
$$\sigma^2_{Y'} = n\sigma^2_X + \sigma^2_E$$

for determining the period jitter of the original signal (σ_X).

3. The circuit of claim 1, wherein the TDC further comprises a latch chain, a counter, an encoder and a set of flip-flops.

4. The circuit of claim 3, wherein the TDC performs operating modes of HOLD, RUN and CLEAR in a single synchronous cycle.

5. The circuit of claim 3, wherein the encoder uses equalization encoding for linearizing the output of the TDC and balancing the difference between rising-time and falling-time of the signal in a standard cell in the latch chains so that enhance measurement precision.

6. The circuit of claim 3, wherein the circuit further comprises a multiplexer and a set of D flip-flops for correcting random output of latch chain and increasing fault coverage.